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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/748,589
Filing Date: December 22, 2000
Appellant(s): MARCH ET AL.

Joseph F. Hetz
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed June 28, 2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 126-134 (Group I), 135 and 139-141 (Group II), 136 (Group III), 137 (Group IV), and 138 (Group V) do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6,321,358 B1	ANDERSON	11-2001
6,208,545 B1	LEEDY	3-2001
6,108,236	BARNETT	8-2000
6,034,882	JOHNSON et al.	3-2000
5,835,396	ZHANG	11-1998
5,708,667	HAYASHI	1-1998

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 126-135 and 138-141 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang, U.S. Patent 5,835,396 (hereinafter "Zhang") in view of Leedy, U.S. Patent 6,208,545 B1 (hereinafter "Leedy"), or alternatively over Johnson, U.S. Patent 6,034,882 (hereinafter "Johnson") in view of Leedy.

As to claims 126 and 128, both Zhang and Johnson each individually teach *a three dimensional write-once memory device including support element carrying a memory array comprising a plurality of cells arranged in a plurality of layers stacked vertically above one another, the memory cell layers deposited, patterned, and etched without using any bonding material between the layers* (see Zhang Abstract, Figs. 1, 4, 5, and 6, and col. 1 lines 14-16 and 63-67, col. 2 lines 1-9 and 16-26, and col. 10 line 49 to col. 11 line 28; see Johnson Abstract,

Figs. 4 and 5, and col. 1 lines 14-60, col. 4 lines 11-22, col. 12 line 42 to col. 13 line 25, col. 16 lines 4-20, and col. 18 lines 32-36; also as admitted by Applicant at page 37 of the response received Dec. 22, 2003, paper no. 35). Neither Zhang nor Johnson disclose *ECC circuitry carried by the support element.* However, such an arrangement is disclosed in the analogous 3-D array of Leedy (see Leedy Background, Fig. 2C, col. 6 lines 61-66, and col. 12 lines 23-31). Clearly the ECC circuitry of Leedy is not specifically required for a 3-D memory with bonded layers, but rather as well known in the art allows for correction of errors which may become more prevalent in any higher density memory circuit, such as any 3-D memory. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to add ECC circuitry to the memories of Zhang and Johnson, because it was known to add this circuitry to the support element of high density 3-D memory arrays so that they could benefit from it's error correction capabilities.

As to claim 130, the prior art combination teaches the method substantially as described above with regard to claim 126; the ECC of Leedy inherently has at least one data bit and one generated ECC bit stored in the array. Evidence of the inherency of storing data and ECC bits when using ECC was previously provided in paper no. 16, page 3 as Barnett, US Patent 6,108,236, at Fig. 6 and at col. 5 lines 28-46, and was not disputed.

As to claim 131, the prior art combination teaches the method substantially as described above with regard to claim 126; it is inherent for ECC

circuitry to retrieve the data and ECC bit as recited and to identify an error, also as evidenced by the Barnett patent cited with regard to claim 130 above.

As to claims 135, 138, and 140, the prior art combination teaches the method substantially as described above with regard to claim 126; any device might be considered releasably coupled to the extent claimed, as previously stated and not disputed.

As to claims 127, 132, 133, and 139, the devices of the above prior art combination may be considered protective housings to the extent claimed. In particular it was previously stated and not disputed that the device of Leedy includes a protective housing, which by definition simply covers, supports, or protects its contents.

As to claims 129, 134, and 141, the devices of the above prior art combination is selected from the recited group since it is semi-conductor based.

Claim 136 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang in view of Leedy, and further in view of Hayashi, U.S. Patent 5,708,667 (hereinafter "Hayashi"), or alternatively over Johnson in view of Leedy, and further in view of Hayashi.

As to claim 136, the Zhang-Leedy or Johnson-Leedy prior art combinations do not disclose that the ECC generator is implemented in software. However, the implementation of ECC in software was well known in the art; Hayashi describes an ECC implemented in software, as shown in Figure 1 and described at column 3 line 11 to column 4 line 13, and at column 7 lines 37-39. An artisan is well aware of the advantages of updatability and adaptability

provided by an implementation in software, and these advantages would have motivated one to implement the ECC of the prior art combination in this manner. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the ECC in software, because this is well known and provides the system adaptability and updatability.

Claim 137 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang in view of Leedy, and further in view of Anderson, U.S. Patent 6,321,358 B1 (hereinafter "Anderson"), or alternatively over Johnson in view of Leedy, and further in view of Anderson.

As to claim 137, the Zhang-Leedy or Johnson-Leedy prior art combinations do not disclose the ECC generator is part of the file system. However, it was well known to incorporate the ECC with the file system for a storage device, see Anderson Figure 31, column 22 line 64 to column 23 line 10, and column 24 lines 37-52. An artisan would have recognized the advantage of compatibility with existing file systems implementing ECC to make the ECC generator part of the file system in the implementation of the device in the prior art combination. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the ECC generator as part of the file system, because this would make of the device of the prior art combination useable with known file systems which incorporate ECC generation.

(11) Response to Argument

With regard to argument VIII. A. Group I (pages 5-8 of the brief):

It is first noted that the Appellants have not disputed the Examiner's contention in the rejections above that Zhang and Johnson both individually teach the recited three dimensional write once memory device including support element carrying a memory array comprising a plurality of cells arranged in a plurality of layers vertically stacked one above another, the memory cell layers deposited, patterned, and etched without any bonding material between the layers. The only additional limitation needed to equal claim 126 is *ECC circuitry carried by the support element.*

The Appellants argue that one skilled in the art would not have been motivated to combine Leedy with either Zhang or Johnson as stated in the rejection, citing *IN RE RATTI* as evidence of such when there must be a substantial reconstruction and redesign, or a resultant change in the basic principle in which one of the references was designed to operate. However, the argument is largely made with respect to why one would have been motivated to modify Leedy in view of Zhang or Johnson (with the exception of the footnote on page 7 of the brief), but the rejection was made with respect to the motivation for modifying Zhang or Johnson in view of Leedy. That is, it is immaterial if (but the Examiner does not agree that) Leedy teaches against fabrication of a multi-layered memory device without using any bonding material between the layers, or that ECC is merely an ancillary feature thereof, the fact remains that Leedy does in fact teach that ECC is advantageously incorporated into the support element of an analogous three-dimensional (multi-layered) memory device, and this teaching is without regard to the method of manufacturing the memory

device layers. Therefore this teaching is applicable to any high density, three dimensional, multi-layered memory device, and thus to the devices of Zhang and Johnson. The footnote at page 7 of the brief states that ECC circuitry adds delays and increases chip size, an undesirable effect for high-density memories, but any disadvantages were obviously not enough to prevent Leedy from incorporating it for their three dimensional high-density memory to achieve the well known aforementioned benefit of error correction capabilities.

Notwithstanding the previous paragraph conclusions, the Examiner argues that Leedy does not teach against the combination in the manner stated by the Appellants. While it is true that Leedy is focused on improving over a conventional two dimensional memory layout, and over existing three dimensional stacks, the manufacturing process described therein does not teach against possible further improvements in such a three dimensional manufacture. In the sections of Leedy cited at page 7 of the brief it is clear that when Leedy states "conventional" and "monolithic", that it is the prior two-dimensional memory to which it is referring; see column 2 lines 31-32 where the prior three-dimensional implementations are described as "conventional" circuits that are stacked. That is, Leedy teaches to implement memory as three-dimensional, or in layers; even if Leedy did not conceive how to implement such a three dimensional circuit monolithically, this does not teach against such an implementation. Additionally, as previously stated in the rejection above the teaching of the use of ECC has nothing to do with whether the device is monolithic; rather it is used because it is a three-dimensional memory and

consequently has a much higher memory density. It is well known in the art that with higher memory density comes the higher likelihood that an error might occur within the device.

It is further noted that the Appellants have not argued the Examiner's rejection of the only additional limitation needed to equal independent claim 130 (*ECC bits are generated and stored in the memory array*).

With regard to argument VIII. B. Group II (pages 8-9 of the brief):

Appellants argue that Leedy teaches ECC circuitry in the memory device, not in a data storage system. It is noted that Appellants have not argued the limitation added to claim 135 (*the memory device is releasably coupled to the data storage system*). The memory device of Leedy makes whatever system it is in a data storage system. A data storage system necessarily includes storage, such storage may include this memory device. Therefore, ECC in the memory device is also in the data storage system. This does not prevent the interpretation that the memory device is releasably coupled to the data storage system, which obviously includes more than one component, any of which may or may not be coupled to the data storage system at any given time.

Appellant's only figure showing any ECC circuitry structure is Figure 11 which shows the circuitry within the memory device. Further, Appellant has for the duration of the prosecution been attempting to convince the Examiner that ECC combined on the same chip with their memory is new. For these reasons, the Examiner interpreted Claim 135 as the data storage system includes the memory device (even though the latter is releasably coupled thereto), and thus

also the ECC functionality; ECC added outside the memory device would have been the conventional implementation. However, even though the specification at page 7 lines 9-15 mentions an embodiment where ECC is implemented outside the memory device, the disclosure's lack of further description of drawings showing such an embodiment indicate that the Appellant considered the off-memory device implementation of ECC to be readily enabled and that those skilled in the art would have known how to implement it as such. Therefore, the Examiner maintains that the general teaching of using ECC with a three-dimensional memory taught by Leedy would have been just as easily been implemented by an artisan with the ECC functionality off of the memory device, since that was the conventional implementation of ECC. Notwithstanding the above, it is further argued that even with the ECC circuitry on the memory device, the data storage system coupled thereto requires "ECC functionality" to the extent claimed to properly utilize and process the corrected data; note the well known ECC circuit of Barnett (US 6,108,236, cited hereinabove) at Fig. 6 which shows the exterior circuitry must be able to process as an example indications that errors have or have not occurred (at 142, 144, and 146, see Barnett col. 6 lines 58-61).

With regard to argument VIII. C. Group III (page 9 of the brief):

Appellants argue that Hayashi does not implement the ECC functionality in software in a data storage system, but rather in the controller or CPU of the memory device. As argued with regard to Group II above, since the memory device and its controller may be considered part of the data storage system, the

ECC is implemented in software in the data storage system; however, even if the memory device is interpreted as separate from the data storage system, the controller or CPU is part of the data storage system (and thus also the software, and the ECC functionality).

With regard to argument VIII. D. Group IV (page 10 of the brief):

Appellants argue that in Anderson the file system information is combined with or embedded in ECC and thus are separately generated. However, the claim merely states that ECC is implemented in a file system, it is noted that the ECC of Anderson is used to reconstruct file system information and thus is implemented in the file system to the extent claimed.

With regard to argument VIII. E. Group V (pages 10-11 of the brief):

Appellants argue that Leedy does not implement the ECC in hardware in a data storage system; see the Group II response above which also applies here.

With regard to argument VIII. F. Claims 126, 130, 135 (page 11 of the brief):

Appellants argue that the claim language "plurality of memory cells arranged in a plurality of layers" is clear. However, the language may be interpreted as 1) "plurality of memory cells, [*each cell*] arranged in a plurality of layers" (that is, "arranged in a plurality of layers" refers to "cells", or 2) (as thought to be intended) "a plurality of layers, [*each layer made up of*] a plurality of memory cells" (that is, "arranged in a plurality of layers" refers to the "plurality" of cells. The claims further recite "the memory cell layers are ..." which might imply

interpretation 1). Examiner requested amendment to prevent the interpretation 1).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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Primary Examiner
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August 5, 2004

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